What is claimed is:

1. An interface circuit for digital signals, comprising:
receiving means for receiving digital signals relative to a first ground potential;
transformer means coupled to the receiving means for passing edges of signals received at the receiving means; and
reconstruction means coupled to the transformer means for reconstructing signals from the edges of signals passed by the transformer means, so as to produce digital signals relative to a second ground potential.

2. The interface circuit according to claim 1 wherein the reconstruction means comprises Schmitt trigger means.

3. The interface circuit according to claim 2 wherein the Schmitt trigger means comprises bias means for biasing the DC level of the edge signals between the trigger levels of the Schmitt trigger means.

4. The interface circuit according to claim 2 wherein the reconstruction means further comprises oscillator means coupled to the Schmitt trigger means for setting the bias point of the Schmitt trigger means to reduce the temperature variability thereof.

5. The interface circuit according to claim 4 wherein the oscillator means comprises a Schmitt trigger arrangement.

6. The interface circuit according to claim 5 wherein the Schmitt trigger means and the Schmitt trigger arrangement are located on the same semiconductor die.

7. An interface circuit for interfacing digital signals to and from a bus, comprising:

first receiving means for receiving digital signals, relative to a first ground potential, for transmission on the bus;

first transformer means coupled to the first receiving means for passing edges of signals received at the first receiving means;

first reconstruction means coupled to the first transformer means for reconstructing signals from the edges of signals passed by the first transformer means, so as to produce digital signals, relative to a second ground potential, for transmission on the bus;

second receiving means for receiving digital signals, relative to the second ground potential, from the bus;

second transformer means coupled to the second receiving means for passing edges of signals received at the second receiving means; and

second reconstruction means coupled to the second transformer means for reconstructing signals from the edges of signals passed by the second transformer means, so as to produce digital signals, relative to the first ground potential, from the bus.

8. The interface circuit according to claim 7 wherein the first and second reconstruction means comprise respectively first and second Schmitt trigger means.

9. A method for interfacing digital signals, comprising:
receiving digital signals relative to a first ground potential;
applying the received digital signals to transformer means to pass edges of the received digital signals; and
reconstructing signals from the signal edges passed by the transformer means so as to produce digital signals relative to a second ground potential.

10. The method for interfacing digital signals according to claim 9 wherein the step of reconstructing comprises applying the signal edges passed by the transformer means to Schmitt trigger means so as to produce digital signals relative to a second ground potential.

11. An interface circuit for digital signals substantially as hereinbefore described with reference to the accompanying drawing.

12. A method for interfacing digital signals substantially as hereinbefore described with reference to the accompanying drawing.